ABSTRACT OF THE INVENTION

An analog delay locked loop for receiving a reference clock signal and for generating a delayed output clock signal includes a voltage controlled delay line, a fixed delay line, a delay voltage control, a fast/slow latch, a phase detector, as well as reset and clock off circuits. The fast/slow latch generates three signals that are received by the delay voltage control: a "latched slow signal", a "latched fast signal", as well as a "latched fast to slow signal". The phase detector generates "go fast" and "go slow" signals that are received by the fast/slow latch. The analog delay locked loop sets the initial delay of the delay line at or near its minimum value on start-up. The delay is then forced to increase from the minimum value until a locking condition is achieved independent of the phase relationship between the reference and delayed clock signals.